REMARKS

The present application was filed on October 9, 2001 with claims 1 through 30. Claims 1 through 30 are presently pending in the above-identified patent application. Claims 1, 10, 19, and 27 are proposed to be amended herein.

In the Office Action, the Examiner rejected claims 1, 10, 19, and 27 under 35 U.S.C. §102(e) as being anticipated by Nakamura et al. (United States Patent Application Number 2002/0099912) and rejected claims 2-9, 11-18, 20-26, and 28-30 under 35 U.S.C. §103(a) as being unpatentable over Nakamura et al.

The present invention is directed to a method and apparatus for adaptively decreasing cache trashing in a cache memory device. Cache performance is improved by automatically detecting thrashing of a set and then providing one or more augmentation frames as additional cache space. In one embodiment, the augmentation frames are obtained by mapping the blocks that map to a thrashed set to one or more additional, less utilized sets. The disclosed cache thrashing reduction system initially identifies a set that is likely to be experiencing thrashing, referred to herein as a thrashed set. Once thrashing is detected, the cache thrashing reduction system selects one or more additional sets to augment a thrashed set, referred to herein as the augmentation sets. In this manner, blocks of main memory that are mapped to a thrashed set are now mapped to an expanded group of sets (the thrashed set and the augmentation sets). Finally, when the augmentation sets are no longer likely to be needed to decrease thrashing, the augmentation set(s) are disassociated from the thrashed set(s).

The specification has been amended to correct typographical errors.

Independent Claims 1, 10, 19 and 27

Independent claims 1, 10, 19, and 27 were rejected under 35 U.S.C. §102(e) as being anticipated by Nakamura et al. In particular, Examiner asserts that the claimed "selector for identifying one or more additional frames" corresponds to circuitry inherently found in Nakamura for selecting/accessing additional sets within cache assist buffer 9, 12 and/or low-level cache memory 11.

Applicant notes that Nakamura discloses an operation that "can transfer line data which has caused thrashing from the cache assist buffer 12 that is *a layer between the level 1 cache memory 23 and the low-level cache memory and main memory*

11." (Page 3, section 39.) Thus, when the cache assist buffer tag 9 has an entry which has a hit in the comparison with the line address for the line data transfer request, *data is transferred from the associated line of the cache assist buffer 12 to the level 1 cache memory 23* as well as to the load and store unit 1 via the data transfer path 13. (Page 3, section 42.) Independent claims 1, 10, 19, and 27, as amended, require wherein said one or more additional frames and said thrashed set are *at the same cache hierarchical level.* It is noted that the "same memory hierarchical level" as said cache includes frames in the same cache or an equivalent memory hierarchical level.

Thus, Nakamura et al. do not disclose or suggest wherein said one or more additional frames and said thrashed set are at the same cache hierarchical level, as required by independent claims 1, 10, 19, and 27, as amended.

Dependent Claims 2-9, 11-18, 20-26 and 28-30

Dependent 2-9, 11-18, 20-26, and 28-30 under 35 U.S.C. §103(a) as being unpatentable over Nakamura et al.

Claims 2-9, 11-18, 20-26, and 28-30 are dependent on claims 1, 10, 19, and 27, respectively, and are therefore patentably distinguished over Nakamura et al. because of their dependency from amended independent claims 1, 10, 19, and 27 for the reasons set forth above, as well as other elements these claims add in combination to their base claim.

All of the pending claims, i.e., Claims 1-30, are in condition for allowance and such favorable action is earnestly solicited.

If any outstanding issues remain, or if the Examiner has any further suggestions for expediting allowance of this application, the Examiner is invited to contact the undersigned at the telephone number indicated below.

The Examiner's attention to this matter is appreciated.

Respectfully submitted,

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